Politecnico di Torino
Dip. di Automatica e Informatica

C.so Duca degli Abruzzi 24
I-10129 Torino TO
Italy

Reviewer's opinion on the Ph.D. dissertation authored by

Sylwester Milewski

entitled

HYPERCOMPRESSION OF TEST DATA

1. Problem and its impact

The dissertation focuses on the test of digital circuits. This issue is crucial both from a scientific and a practical point of view, since the ability to adequately test electronic circuits with minimal effort and cost strongly impacts their quality and market success.

In particular, the dissertation deals with the techniques for testing digital circuits resorting to Design for Testability (DfT), and aims at advancing the state of the art by reducing the test duration and hardware overhead. The dissertation proposes several techniques which are able to reduce the amount of test vectors to be applied to the circuit to achieve a given stuck-at fault coverage, thus reducing correspondingly the duration (and hence the cost) of the test. The proposed techniques appear to advance the state of the art with respect to both the scientific literature and the commercial software suites on the market. Hence, their practical relevance is out of discussion.

2. Contribution

The dissertation provides three major contributions with respect to the state of the art:

- a stand-alone method to reduce the number of test vectors required to achieve a given fault coverage (Chapter 4); the method is based on grouping faults into clusters of likely compatible faults, based on the results of the fault simulation of previously ATPG generated patterns. A SAT-based ATPG is then launched to generate a single test pattern per cluster, thus creating a significantly compacted test set.
- a new method, named *hypercompression* (Section 5), which builds on the isometric compression paradigm, but makes it more flexible by allowing to select the full-toggle scan chains; in such a way the method achieves unprecedented encoding efficiency and guarantees extremely high test coverage with a hardware cost which is still comparable with that of previous solutions.
- the adoption of hypercompression to support low-power constraints (Section 6). In this case a lower power consumption during test is considered as a target, and

Matteo SONZA REORDA *Tel.:* +39 011 090.7055 *matteo.sonzareorda*@polito.it
Fax: +39 011 090.7099

C.so Duca degli Abruzzi 24
I-10129 Torino TO
Italy

the hardware architecture is modified accordingly. This new architecture also shows the flexibility of the hypercompression solution.

In all the above cases, the candidate clearly described the proposed techniques and proved experimentally their effectiveness on a reasonable set of benchmark circuits.

However, in my opinion the overall main contribution of the dissertation lies in proving that a well integrated approach linking the ATPG and the DfT hardware generator can allow a significant reduction in the test time, thanks to a reduced number of test vectors optimally suiting to be embedded in the DfT hardware. A remarkable point in the dissertation corresponds to the description of the hypercompression hardware architecture, but also in highlighting how to optimally adapt the ATPG process to produce the inputs for designing such an architecture, achieving an optimal trade-off between test time and hardware overhead (or power consumption).

I would also like to emphasize that the experimental results gathered and reported to assess the effectiveness of the proposed techniques did require an extensive work combining different tools and running them on real-world benchmark circuits. This further proves how well the candidate masters techniques and tools in the domain.

I'm also impressed by the number and quality of the papers published by the candidate (although only some of them are mentioned in the dissertation). This further witnesses the importance of his contribution to the state of the art in the area.

3. Correctness

I couldn't find any flaw in the dissertation. The state of the art as well as the proposed techniques are correctly and clearly presented, as well as the experimental results showing their effectiveness.

I have only a few small comments targeting possible improvements in the dissertation document

1. The candidate never mentioned the computational time required by the ATPG and the other tools to perform their task. Although I guess that this time is perfectly acceptable, it would be nice to report some figures about it and about the scalability of the methods.
2. In some cases I would suggest adding some more discussion about the reported results. For example
    a. In section 4.3 the available test patterns are divided in two groups G_1 and G_2. It would be nice to better explain how the threshold distinguishing G_1 from G_2 has been selected, as well as discussing the impact that the value of this threshold may have on the method effectiveness (if any).

Matteo SONZA REORDA *Tel.:* +39 011 090.7055 *matteo.sonzareorda*@polito.it
Fax: +39 011 090.7099

C.so Duca degli Abruzzi 24
I-10129 Torino TO
Italy

b. In section 5.4 it is shown that the proposed method gives different results in terms of TP reduction depending on the circuits. Why? Is this related to the circuit or to the starting TPs? In fact, it seems that the achieved TP reduction is inversely proportional to the initial FC. Some more discussion about this point would be useful.
c. Results about transition faults (Table 5.4) are a bit vague. Did the experiments performed to gather the above results use the LOC scheme? How the hypercompression architecture should be modified to test transition faults?

3. As far as I understood, most of the dissertation focuses on stuck-at faults. It would be nice to know how the proposed techniques can possibly extend to other fault models as well. For example, are the proposed techniques suitable to also manage the case where Cell-Aware Test is adopted?

4. Knowledge of the candidate

Section 1 introduces the work done in the dissertation, while Sections 2 and 3 summarize the state of the art in the area covered by the dissertation (i.e., test of digital circuits via scan and logic BIST) and set up the required background material. All the relevant papers are properly mentioned in these sections as well as in the others composing the dissertation. The whole dissertation is clear, complete and nicely written, showing that the candidate masters very well the domain.

Matteo SONZA REORDA *Tel.:* +39 011 090.7055 *matteo.sonzareorda*@polito.it
Fax: +39 011 090.7099

Politecnico di Torino
Dip. di Automatica e Informatica

C.so Duca degli Abruzzi 24
I-10129 Torino TO
Italy

5. Conclusion

Taking into account what I have presented above and the requirements imposed by Article 13 of *the Act of 14 March 2003 of the Polish Parliament on the Academic Degrees and the Academic Title* (with amendments), my evaluation of the dissertation according to the three basic criteria is the following:

A. Does the dissertation present an original solution to a scientific problem? (the selected option is marked with **X**)

[**X**]	[ ]	[ ]	[ ]	[ ]
Definitely YES	*Rather yes*	*Hard to say*	*Rather no*	*Definitely NO*

B. After reading the dissertation, would you agree that the candidate has general theoretical knowledge and understanding of the discipline of **Information and Communication Technology**, and particularly the area of **digital circuit testing**?

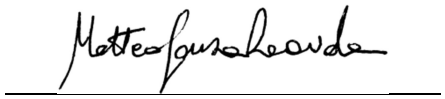
[**X**]	[ ]	[ ]	[ ]	[ ]
Definitely YES	*Rather yes*	*Hard to say*	*Rather no*	*Definitely NO*

C. Does the dissertation support the claim that the candidate is able to conduct scientific work?

[**X**]	[ ]	[ ]	[ ]	[ ]
Definitely YES	*Rather yes*	*Hard to say*	*Rather no*	*Definitely NO*

Moreover, taking into account the quality of the performed work and of the dissertation, I **recommend to distinguish** the dissertation for its quality.

Torino, January 3, 2022



prof. Matteo Sonza Reorda,
PhD and IEEE Fellow

Matteo SONZA REORDA *Tel.:* +39 011 090.7055 *matteo.sonzareorda*@polito.it
Fax: +39 011 090.7099